IN THE SPECIFICATION:

Please amend paragraph **[0004]** as follows:

[0004] Display devices visually present information generated by computers and other electronic devices. One category of display devices is electron emitter apparatus, such as a cold cathode field emission display (FED). ~~A FED~~ An FED uses electrons originating from one or more emitters on a baseplate (also known as the panel) to illuminate a luminescent display screen and generate an image. The emitters can be arranged in groups called pixels. A gate electrode, located near the emitter, and the baseplate are in electrical communication with a voltage source. Electrons are emitted when a sufficient voltage differential is established between the emitter and the gate electrode. The electrons strike a phosphor coating on the display screen, releasing photons to generate a visual image.

Please amend paragraph **[0006]** as follows:

[0006] High resolution displays yield brighter images on the display screen and are therefore in high demand. High resolution displays may be obtained by creating a focused electron beam which reduces off-angle beams and mislanded electrons and therefore yields a brighter image. One method of obtaining such a focused electron beam is to fabricate emitters with substantially similar heights. The voltage ~~then~~ is then applied to a gate electrode and such emitters ~~extracts~~ extract a high number of electrons since the distance between the gate electrode and the emitter is uniform. If the height of the emitters is not uniform throughout the panel, the distance between the gate electrode and the emitters can vary from one emitter to the next. When this occurs, the number of electrons and the direction of emission vary, yielding a dimmer image because fewer electrons strike the display screen in the same area.

Please amend paragraph **[0007]** as follows:

[0007] A problem with conventional emitters arrayed on a panel has been the ~~non-uniformity~~ non-uniformity of the emitter height. Emitters are often longer in the interior of the panel and shorter in the periphery of the panel because of etching reactor design and etching reactor loading of panels. The design of etching reactors causes slower etching in the interior of

the panel and quicker etching in the periphery of the panel. Etching reactor loading -- where etching is slower in the interior of the reactor because the etching process occurs in all directions and faster in the periphery of the reactor, especially the edges, because the etching does not occur in all directions -- also contributes to this non-uniformity. This non-uniformity of the emitter height, as discussed above, has contributed to dimmer images.

Please amend paragraph **[0015.2]** as follows:

[0015.2] FIG. 11 illustrates the distribution of emitter heights according to an embodiment of the present invention.

Please amend paragraph **[0016]** as follows:

[0016] The present invention provides a method for enhancing the uniformity of emitters in display devices. The enhanced emitter uniformity is obtained by using an etch mask with a controlled distribution of mask sizes. The etch mask contains larger mask sizes primarily in the periphery and smaller mask sizes primarily in the interior to compensate for the ~~non-uniform~~ non-uniform etching during formation of the emitters.

Please amend paragraph **[0019]** as follows:

[0019] Illustrated in drawing FIG. 3 is a cross-sectional view ~~of a~~ of an FED 10 containing emitters manufactured according to the present invention. In drawing FIG. 3, substrate 11 comprises any suitable material, such as glass or a ceramic material. Substrate 11 may also be made from other materials such as silicon, optionally with a glass layer deposited thereon. Preferably, a glass panel serves as substrate 11. Conducting layer 12 is disposed on substrate 11. Any conductive material, such as metals or metal alloys, can be used as conducting layer 12. Preferably, conducting layer 12 is a metal, such as aluminum, or an alloy or compound thereof.

Please amend paragraph **[0020]** as follows:

[0020] Emitter 13 is positioned on substrate 11 and conducting layer 12. Emitter 13 serves as a cathode conductor, and although any shape providing the necessary emitting properties can be used, a conical shape is preferred. Emitter 13 may comprise any emitting material, and preferably comprises a low work function material, i.e., a material which requires little energy to emit electrons, coated on the tip. Low work function materials include noble materials such as Mb, Si, cermet ($Cr_3Si + SiO_2$), cesium, nitride metals, niobium, and ~~diamond-like~~ diamond-like carbon. The low work function material is preferably coated on the emitter tip.

Please amend paragraph **[0021]** as follows:

[0021] Surrounding emitter 13 is gate electrode 15. Gate electrode 15 is formed of a conductive material, such as aluminum (Al), tungsten (W), chromium, or molybdenum. Preferably, the gate electrode comprises aluminum (Al). When a voltage differential is applied between emitter 13 and gate electrode 15, a stream of electrons in the form of beam 17 is emitted toward display screen 16 (serving as an anode) with phosphor coating 18. Insulating layer 14 is disposed between conducting layer 12 and gate electrode 15. Any insulating material may be used as insulating layer 14, such as silicon nitride or silicon oxide. Insulating layer 14 flanks ~~emitter tip~~ emitter 13.

Please amend paragraph **[0022]** as follows:

[0022] ~~A FED~~ An FED containing the emitters of the present invention can be formed by many processes, including the process described below and illustrated in FIGS. 4 through 8. First, conducting layer 12 is formed on substrate 11. Conducting layer 12 may be formed by any suitable process, such as one which does not degrade substrate 11. Preferably, conducting layer 12 is deposited by a sputtering process, such as sputtering the selected metal in a vacuum containing argon (Ar). The thickness of conducting layer 12 can range from about 0.1 microns to about 0.6 microns, and is preferably about 0.3 microns.

Please amend paragraph **[0026]** as follows:

[0026] Next, selective portions of mask layer 22 which are not covered by the photoresist pattern are removed, resulting in etch masks 21, which are of a similar pattern as photoresist masks 25. Selective removal of mask layer 22 is accomplished preferably through a dry plasma etch, but any suitable isotropic etching technique can be employed. In this plasma etch method, the etchants used to etch the preferred silicon oxide mask layer 22 include, but are not limited to, halogen gases, such as chlorine or fluorine, and gases containing fluorine, such as CF_4, CHF_3, C_2F_6, and C_3F_6. Other gases, such as argon (Ar), can be included in the plasma atmosphere. The etchant gases selectively etch silicon oxide without removing photoresist ~~mask~~ masks 25. Photoresist masks 25 are then removed by any suitable method known in the art. The resulting structure, as illustrated in drawing FIG. 6, contains etch masks 21 of mask layer 22 material (e.g., silicon oxide) overlying ~~emitter~~ emitting layer 20.

Please amend paragraph **[0030]** as follows:

[0030] The preferred method of obtaining the controlled distribution of emitter sizes is described below. In the preferred method, at least one desired emitter size is first selected and, preferably, a single desired emitter size is selected. The desired size of the emitter depends on numerous factors, such as the type of display device, the material used in emitting layer 22, the conducting material used in the gate electrode, the voltage potential between the extraction electrode and the emitter, and the operating voltage of the anode. For example, in one type of ~~a FED~~ an FED device, the desired emitter size could range from about 0.5 microns to about 1.8 microns. Preferably, the single, desired emitter size in the present invention ranges from about 1.5 microns to about 1.7 microns, ~~and~~ and is preferably 1.6 microns.

Please amend paragraph **[0031]** as follows:

[0031] Next, referring to Figure 10, a controlled distribution of mask sizes is determined. The controlled distribution of ~~mask sizes 21~~ etch mask 21 sizes is selected so that when emitting layer 20 is etched, the controlled distribution of ~~emitter sizes 13,~~ emitter 13 sizes, including the at least one desired emitter size throughout the panel, is formed, as shown in

Figure 11. The controlled distribution of mask sizes depends in part on the number and size of etching areas (e.g., the periphery and the interior) and the number of different mask sizes to be employed.

Please amend paragraph **[0033]** as follows:

[0033] Likewise, the number of mask sizes should be minimized since the more mask sizes that are chosen, ~~the larger the~~ a larger number of different emitter sizes in the display device ~~that will~~ will result. The number of mask sizes must be a plurality, and preferably is an odd number with an equal number of mask sizes larger and smaller than a median mask size. The factors which must be considered are the total number of emitters in a pixel and the uniformity of the etching of the reactor etcher used.

Please amend paragraph **[0037]** as follows:

[0037] Emitters 13 are then formed by emitting layer 20 as described above. As illustrated in drawing FIG. 9, the above process creates a controlled distribution of emitter sizes similar to a curve, with the largest area under the curve having the desired emitter size. Conventional methods, where the emitter height differs between the interior and periphery of the panel, yields a line rather than a curve. Preferably, the above process should be adjusted so that the curve is as flat as possible, thereby maximizing the uniformity of the emitter height. Preferably, the emitter size of all emitters in the FED ranges from about 1.5 microns to about 1.7 microns, ~~and~~ and is more preferably about 1.6 microns. Preferably, the emitter height should be within about 0.5 microns to about 1.5 microns (about 3.25% to about 9.5%) of each other, ~~and~~ and is more preferably about 1.0 microns (about 6 %) of each other.

Please amend paragraph **[0038]** as follows:

[0038] Further processing can then be undertaken to form the remainder of the FED. For example, a low work function material may be formed on the tips of emitters 13; insulating layer 14 and gate electrode ~~layer~~ 15 may be formed; and substrate 11 containing emitters 13 sealed together with the display screen.

Please amend paragraph **[0040]** as follows:

[0040] In a process of fabricating ~~a FED,~~ an FED, emitting layer 20 was formed of amorphous Si and masking layer 22 was formed of silicon oxide on a panel. The desired emitter size for the FED was 1.6 microns. To create a mask pattern, the 3 etching areas and 5 mask sizes were selected. Given the etching parameters for forming amorphous silicon emitters, as described below, the periphery of the mask contained mask sizes of 1.6, 1.7, and 1.8 microns, the middle portion of the mask contained mask sizes of 1.5, 1.6, and 1.7 microns, and the interior of the mask contained mask sizes of 1.4, 1.5, and 1.6 microns. After etching using a suitable known etching process, the periphery of the panel contained an emitter height of 1.4 microns, 1.5 microns, and 1.6 microns, the middle portion of the panel contained an emitter height of 1.5 microns, 1.6 microns and 1.7 microns, and the interior of the panel contained an emitter height of 1.5 microns, 1.6 microns and 1.7 microns, yielding the desired emitter height of 1.6 microns throughout the panel.

Please amend paragraph **[0041]** as follows:

[0041] While the preferred embodiments of the present invention have been described above, the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof. For example, although the method of the invention has been described as forming an emitter array for ~~a FED,~~ an FED, the skilled artisan will understand that the process and emitter array described above can be used for other display devices, such as plasma displays and flat cathode ray tubes.